REMARKS

Claim 1 has been currently amended. Claims 2 and 4-6 were canceled previously. Claims 10-17 have been withdrawn. Claims 1, 3, and 7-18 thus remain pending in the application.

Claim Rejections Under 35 U.S.C. § 103

The Office Action rejects claims 1, 3, 7, 9, and 18 under 35 U.S.C. § 103(a) as being unpatentable over Goldberg et al. (U.S. Patent No. 5,201,046, hereinafter "Goldberg") in view of Roge et al. (U.S. Patent No. 6,721,202, hereinafter "Roge") and further in view of Kay et al. (U.S. Patent No. 6,349,274, hereinafter "Kay"); and rejects claim 8 under § 103(a) as being unpatentable over Goldberg in view of Roge and Kay, as applied to claims 1, 3, 7, 9, and 18, and further in view of Upton (U.S. Patent 7,080,092, hereinafter "Upton").

Applicant disagrees with the above rejections because each of independent claims 1 and 18 recites one or more limitations that are neither taught nor suggested in any of the cited references.

Claim 1. Currently amended claim 1 recites, among other things, the limitation "wherein the read engine operates by reading data from a location in memory and comparing the contents of the memory location with a search object, the read engine using differential bits between the contents of the memory location and the search object to retrieve addresses that point to subsequent memory locations in the database."

The Office Action asserts that the above-quoted limitation is taught by Roge at col. 5, lines 65-67, and col. 6, lines 9-18. These portions of Roge describe the operation of a content-addressable memory circuit that includes "differential bit lines" and "differential compare lines," but Roge says nothing about "using differential bits between the contents of the memory location and the search object to retrieve *addresses* that point to *subsequent* memory locations in the

database" (emphasis added). The cited portions of Roge do not mention any memory location other than the specific one being accessed through the current read, compare, or write operation. Therefore there is no teaching in Roge regarding "subsequent memory locations," as recited in claim 1. To further clarify claim 1, the language "to retrieve addresses that point to" has been added to the claim in place of "locate." Roge is silent regarding the retrieval of addresses that point to subsequent memory locations.

There is ample support for the current amendment to claim 1 in, e.g., Para. 0012 of the specification. No new matter has been introduced via the current amendment of claim 1.

Claim 1 also recites the limitation "wherein the graph engine is implemented entirely in hardware." The Office Action asserts that this limitation is taught in the Abstract of Kay. This is incorrect, however. The Abstract of Kay says nothing whatsoever about a "graph engine" or anything else that could be construed as equivalent to a graph engine as described and claimed in the instant application. In fact, the words "graph" and "engine" appear nowhere in Kay, and the subject matter of Kay is quite distinct from that of the instant application, Kay dealing with a configuration manager for configuring a data acquisition system. Moreover, the Abstract of Kay says nothing about anything being implemented "entirely in hardware," let alone a "graph engine," as recited in claim 1.

Claim 1 also recites the limitation, "wherein the entire database resides in one of random-access memory and flash memory." The Office Action asserts that this is also taught in the Abstract of Kay. Kay does discuss a "hardware database 210," but that cannot meet the just-quoted limitation of claim 1 for at least a couple of reasons. First, the "hardware database 210" in Kay is not a database that is implemented in hardware. Rather, hardware database 210 is a *software-implemented* database that stores information *about* hardware (e.g., cards or boards) in

the described data acquisition system (see Kay, col. 7, lines 35-38). Second, Kay's hardware database 210 is stored in a "nonvolatile memory or hard drive 162." Clearly, a "hard drive" (a magnetic-disk storage device) is neither random-access memory (RAM) nor flash memory. Therefore, Kay does not teach that "the entire database resides in one of random-access memory and flash memory," as recited in claim 1.

Because currently amended claim 1 recites limitations that are not taught or suggested in Goldberg, Roge, or Kay, whether considered separately or in combination, claim 1 is not rendered obvious by those references under § 103(a), and Applicant believes currently amended claim 1 to be allowable. Each of dependent claims 3 and 7-9 is thus also allowable, at least by virtue of its depending from allowable claim 1. Withdrawal of the rejections of claims 1, 3, and 7-9 under § 103(a) is respectfully requested.

Claim 18. Claim 18 also recites, among other things, the limitations "wherein the graph engine is implemented entirely in hardware" and "wherein the entire database resides in one of random-access memory and flash memory." The Office Action applies the same references and arguments against these limitations as it does against the similar limitations in claim 1. Therefore, arguments similar to those above in connection with claim 1 also apply to claim 18. Withdrawal of the rejection, under § 103(a), of claim 18 is respectfully requested.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that no further impediments exist to the allowance of this application and, therefore, requests an indication of allowability. However, the Examiner is requested to call the undersigned if any questions or comments arise.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-1283.

COOLEY GODWARD KRONISH LLP
ATTN: Patent Group
777 6th Street NW, Suite 1100
Washington, DC 20001
Tel: (720) 566-4044
Fax: (202) 842-7899

Respectfully submitted,
COOLEY GODWARD KRONISH LLP

By: Thomas M. Croft

Thomas M. Croft
Reg. No. 44,051